Remarks

The Office Action dated January 23, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 11, 14, 17-19, 21 and 24-26 have been amended. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Claims 30-48 were withdrawn from consideration. Accordingly, claims 1-29 are pending in the present application. Claims 1-13, 15 and 16 have been allowed. Claims 14 and 17-29 are respectfully submitted for reconsideration.

Claims 24 and 25 were objected to because of the informalities. Claims 24 and 25 are formally amended. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection to claims 24 and 25.

Claims 14 and 17-29 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 14,17-19, 21, 24-26 have been amended to more clearly recite the claimed invention. Therefore, claims 14 and 17-29 are in compliance with U.S. Patent Practice.

Claims 18, 22-25, 28 and 29 were rejected under 35 U.S.C. §102(b) as being anticipated by Akiyama, Hideki (JP-05053857 A). Applicant respectfully submits that each of claims 18, 22-25, 28 and 29 recites subject matter that is neither disclosed nor suggested in this cited prior art.

Claim 18, as amended, recites an electronic device having first and second semiconductor devices connected to each other with a plurality of bus lines. The first semiconductor device includes a first output circuit connected to one of the plurality of bus lines for supplying the bus line with a first logical output signal, an inversion output circuit connected to the bus line for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the bus line with the first logical output signal, and a comparison circuit connected to the bus line. The second semiconductor device includes an input circuit connected to the bus line for acquiring a first bus line signal, and a second output circuit connected to the input circuit for supplying the bus line with the first bus line signal. The comparison circuit receives a second bus line signal from the bus line and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

Accordingly, Claim 18 presupposes a "bus line", through which the "first logical output signal", "second logical output signal" and "first bus line signal" are propagated from the first semiconductor device to the second semiconductor device, and also the "first bus line signal" and "second bus line signal" are propagated from the second semiconductor device to the first semiconductor device. At least one of the essential features of claim 18 is an "inversion output circuit" connected to the bus line for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the bus line with the first

logical output signal. At least another one of the essential features of claim 18 is a "comparison circuit" that is connected to the bus line and receives a second bus line signal from the bus line and compares the first logical output signal and the second bus line signal. As such, at least one of the advantages of claim 18 is that the residual charges on the bus line can be removed before the second semiconductor device supplies the bus line with the first bus line signal. At least another one of the advantages of claim 18 is that the comparison circuit can detect the drive capability upon the bus line of the second semiconductor device.

It is respectfully submitted that Akiyama fails to disclose or suggest the elements of the present invention as set forth in claim 18, and therefore fails to provide the advantage that are provided by the present application.

Akiyama discloses a bus line (103) through which data is propagated from LSI-A (10) to LSI-B (20), and another bus line (104) through which data is propagated from LSI-B (20) to LSI-A (10). Therefore, Akiyama fails to disclose or suggest the "bus line" through which the "first logical output signal", "second logical output signal" and "first bus line signal" are propagated from the first semiconductor device to the second semiconductor device, and also the "first bus line signal" and "second bus line signal" are propagated from the second semiconductor device to the first semiconductor device, as is the presupposition of claim 18.

Akiyama merely discloses an input buffer (1), which supplies an internal wring (105) in the LSI-A (10) with an inverted signal. The internal wiring (105) of Akiyama is not a bus line (103). The data supplied from the input buffer (1) is stored in the test data

register (2). (Please refer to the column [0014] of the English translation of Akiyama that was submitted on August 7, 2003). Therefore, Akiyama fails to disclose or suggest the "inversion output circuit" connected to the bus line for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the bus line with the first logical output signal, as recited in claim 18.

Furthermore, Akiyama discloses a comparator (5), which compares data from the test data register (2) in the LSI-A (10) with data from the comparison register (4) in the same LSI-A (10). Therefore, Akiyama fails to disclose or suggest the "comparison circuit" that is connected to the bus line and receives a second bus line signal from the bus line and compares the first logical output signal and the second bus line signal, as recited in claim 18.

Accordingly, Applicant submits that Akiyama fails to disclose or suggest each and every element recited in claims 18 of the present application, and that claim 18 is allowable.

Claim 24, as amended, recite a first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto with a plurality of bus lines. The first semiconductor device includes an output circuit connected to one of the plurality of bus lines that supplies the bus line with a first logical output signal. The second semiconductor device receives a first bus line signal from the bus line and supplies the bus line with a second logical output signal being an inverted signal of the first bus line signal. The first semiconductor device also

includes a comparison circuit connected to the bus line that receives a second bus line signal from the bus line and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device.

Accordingly, Claim 24 presupposes a "bus line", through which the "first logical output signal" and "first bus line signal" are propagated from the first semiconductor device to the second semiconductor device, and also the "second logical output signal" and "second bus line signal" are propagated from the second semiconductor device to the first semiconductor device. At least one of the essential features of claim 24 is a "second semiconductor device" which receives a first bus line signal from the bus line and supplies the bus line with a second logical output signal being an inverted signal of the first bus line signal. At least another one of the essential features of claim 24 is a "comparison circuit" that is connected to the bus line and receives a second bus line signal from the bus line and compares the first logical output signal and the second bus line signal. As such, at least one of the advantages of claim 24 is that the residual charges on the bus line can be removed when the second semiconductor device supplies the bus line with the second logical output signal being an inverted signal of the first bus line signal. At least another one of the advantages of claim 24 is that the comparison circuit can detect the drive capability upon the bus line of the second semiconductor device.

It is respectfully submitted that Akiyama fails to disclose or suggest the elements of the present invention as set forth in claim 24, and therefore fails to provide the advantage that are provided by the present application.

Akiyama discloses a bus line (103) through which data is propagated from LSI-A (10) to LSI-B (20), and another bus line (104) through which data is propagated from LSI-B (20) to LSI-A (10). Therefore, Akiyama fails to disclose or suggest the "bus line" through which the "first logical output signal" and "first bus line signal" are propagated from the first semiconductor device to the second semiconductor device, and also the "second logical output signal" and "second bus line signal" are propagated from the second semiconductor device to the first semiconductor device, as is the presupposition of claim 24.

Akiyama merely discloses LSI-B (20), which receives data from a bus line (103) and supplies another bus line (104) with said data. The selector (7) of Akiyama does not invert the data. (Please refer to the column [0010] of the English translation of Akiyama that was submitted on August 7, 2003). Therefore, Akiyama fails to disclose or suggest the "second semiconductor device" which receives a first bus line signal from the bus line and supplies the bus line with a second logical output signal being an inverted signal of the first bus line signal, as recited in claim 24.

Furthermore, Akiyama discloses a comparator (5), which compares data from the test data register (2) in the LSI-A (10) with data from the comparison register (4) in the same LSI-A (10). Therefore, Akiyama fails to disclose or suggest the "comparison circuit" that is connected to the bus line and receives a second bus line signal from the

bus line and compares the first logical output signal and the second bus line signal, as recited in claim 24.

Accordingly, Applicant submits that Akiyama fails to disclose or suggest each and every element recited in claims 24 of the present application, and that claim 24 is allowable.

Claim 25, as amended, recites a first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto with a plurality of bus lines. The first semiconductor device includes an output circuit connected to one of the plurality of bus lines that supplies the bus line with a first logical output signal. The second semiconductor device receives a first bus line signal from the bus line and supplies the bus line with the first bus line signal. The first semiconductor device also includes an inversion output circuit connected to the bus line that supplies the bus line with a second logical output signal being an inverted signal of the first logical output signal after the output circuit supplies the first logical output signal, and a comparison circuit connected to the bus line that receives a second bus line signal from the bus line and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding the connection between the first semiconductor device and the second semiconductor device.

Accordingly, Claim 25 presupposes a "bus line", through which the "first logical output signal", "second logical output signal" and "first bus line signal" are propagated from the first semiconductor device to the second semiconductor device, and also the "first bus line signal" and "second bus line signal" are propagated from the second

semiconductor device to the first semiconductor device. At least one of the essential features of claim 25 is an "inversion output circuit" connected to the bus line that supplies the bus line with a second logical output signal being an inverted signal of the first logical output signal after the output circuit supplies the bus line with the first logical output signal. At least another one of the essential features of claim 25 is a "comparison circuit" that is connected to the bus line and receives a second bus line signal from the bus line and compares the first logical output signal and the second bus line signal. As such, at least one of the advantages of claim 25 is that the residual charges on the bus line can be removed before the second semiconductor device supplies the bus line with the first bus line signal. At least another one of the advantages of claim 25 is that the comparison circuit can detect the drive capability upon the bus line of the second semiconductor device.

It is respectfully submitted that Akiyama fails to disclose or suggest the elements of the present invention as set forth in claim 25, and therefore fails to provide the advantage that are provided by the present application.

Akiyama discloses a bus line (103) through which data is propagated from LSI-A (10) to LSI-B (20), and another bus line (104) through which data is propagated from LSI-B (20) to LSI-A (10). Therefore, Akiyama fails to disclose or suggest the "bus line" through which the "first logical output signal", "second logical output signal" and "first bus line signal" are propagated from the first semiconductor device to the second semiconductor device, and also the "first bus line signal" and "second bus line signal"

are propagated from the second semiconductor device to the first semiconductor device, as is the presupposition of claim 25.

Akiyama merely discloses an input buffer (1), which supplies an internal wring (105) in the LSI-A (10) with an inverted signal. The internal wiring (105) of Akiyama is not a bus line (103). The data supplied from the input buffer (1) is stored in the test data register (2). (Please refer to the column [0014] of the English translation of Akiyama that was submitted on August 7, 2003). Therefore, Akiyama fails to disclose or suggest the "inversion output circuit" connected to the bus line that supplies the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the bus line with the first logical output signal, as recited in claim 25.

Furthermore, Akiyama discloses a comparator (5), which compares data from the test data register (2) in the LSI-A (10) with data from the comparison register (4) in the same LSI-A (10). Therefore, Akiyama fails to disclose or suggest the "comparison circuit" that is connected to the bus line and receives a second bus line signal from the bus line and compares the first logical output signal and the second bus line signal, as recited in claim 25.

Accordingly, Applicant submits that Akiyama fails to disclose or suggest each and every element recited in claims 25 of the present application, and that claim 25 is allowable.

As for claims 22, 23, 28 and 29, it is submitted that each of claims 22, 23, 28 and 29 is dependent on claim 18. Thus, Applicant respectfully submits that claims 22, 23, 28 and 29 are allowable due to their dependency from allowable claim 18.

Accordingly, Applicant respectfully request reconsideration and withdrawal of the rejection of claims 18, 22-25, 28 and 29 under 35 U.S.C. §102(b).

Conclusion

Applicant's amendments and remarks have clearly overcome the rejections set forth in the Office Action dated January 23, 2004. Applicant's remarks have distinguished claims 18, 22-25, 28 and 29 from Akiyama and thus overcome the rejection of these claims under 35 U.S.C. §102(b). Accordingly, claims 14 and 17-29 are in condition for allowance. Therefore, Applicants respectfully request reconsideration and allowance of claims 14 and 17-29.

Applicant submits that the application is in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicant respectfully requests that the Examiner contact the undersigned attorney by telephone, if it is believed that such contact will expedite the prosecution of the application.

In the event that this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fee

deficiency or credit any overpayment to Deposit Account No. 01-2300, referencing attorney docket number 108075-09034.

Respectfully submitted,

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Enclosures: Petition for Extension of Time (3 months)